REMARKS

Reconsideration and allowance of the above identified application, as currently amended, is respectfully requested.

By the above amendments, claims 1-8 remain pending, of which claims 1, 2 and 8 were amended. The amendments made to the claims are in consideration of further highlighting the set forth featured aspects in these claims.

In view of the amendments made to the claims, the outstanding objection (see Section 1 on page 2 of the Official Action) was rendered moot. In particular, the first and second frequencies associated with the "first circuits" and "second circuits" of the "second semiconductor chip", which is mounted over the top surface of the printed wiring board, are now specifically defined as being "distinct" from each other. Moreover, the set forth "first semiconductor chip", which is disposed to overlie the "second semiconductor chip" and includes "a first circuit and a second circuit", was further defined such that the "first circuit is independent of the second circuit of the first semiconductor chip." Such is now featured in independent claim 1. Added language of a similar nature has also been effected with regard to claim 2 (dependent on claim 1) to take into account the additional set forth circuits and related operating frequencies thereof. With regard to independent claim 8, the revisions therein are similar to that effected with regard to base claim 1.

In connection with the embodiment shown in Fig. 1+, as one example embodiment of the present invention, although not limited thereto, a power amplifier module 1 is shown in which lower chip 7 represents the "second semiconductor chip", which is mounted over the printed wiring board, and the upper chip 2 is an

example of the set forth "first semiconductor chip" which overlies the lower, "second semiconductor chip."

With regard to claims 1+, for example, the illustrations in Figs. 5-6(see also Figs.7-10) are representative examples thereof, although not limited thereto. Namely, the placement of the amplifier circuits 2c and 2d of the upper chip 2, which are examples of the "first circuit" and the "second circuit" of the set forth "first semiconductor chip", respectively, and which is mounted over a lower chip 7 in Fig. 5, in which the set forth "second circuits" are represented by the left side amplifier circuits 7f, 7g of chip 7 while the right side amplifier circuits thereof, i.e., 7c, 7d, relate to the set forth "first circuits" of the lower, "second semiconductor chip" of the mounted structure, is an example showing of such mounting structure. When the upper chip 2 is mounted over the lower chip 7, the arrangement of the circuits are such that the "first circuit" (e.g., 2c in Fig. 6) is disposed on the same side of the mounting structure so that it is opposite the "second circuits" (e.g., 7f, 7g) of the lower chip 7. Correspondingly, the "second circuit" (e.g., 2d in Fig. 6) is disposed on the same side opposite that of the "first circuits" (e.g., 7c, 7d in Fig. 5) of the lower chip 7. In accordance with the above scheme, high frequency interference caused by wires bonded to the upper chip 2 and the lower chip 7 is prevented. Extensive discussion regarding this is given on page 14, line 15, to page 16, line 10, of the Substitute Specification (corresponding to page 18, line 6, to page 20, line 13, in the original Specification). By effecting a multi-chip mounting structure such as a power amplifier module in which different chips associated therewith have circuits that operate on different frequencies / different timings, for example, a scheme as that

presently set forth prevents interference resulting from occurrences of high frequencies caused by the presence of the bonding wires between that of the upper and lower chips. The circuitry layout in conjunction with the mounting of the first and second chips avoids such concerns, among others. It is submitted, the invention as currently set forth in claims 1-8 is patentable over that previously known including over the art documents as applied thereto in the related rejections.

According to the outstanding Office Action, claims 1, 4, 6 and 7 stand rejected under 35 USC §103(a) over the combination of Kamikuri et al (USP 6,563,206) in view of Winslow et al (USP 6,803,817); claim 2 stands rejected under 35 USC §103(a) over the same combination of Kamikuri et al and Winslow et al and further in view of Hashemi et al (USP 6,674,337); and claims 1, 5 and 8 -13 stand rejected over the combination of Lo et al (USP 6,414,384) in view of Winslow et al. As will be shown below, in conjunction also with the above discussion, the invention according to the currently pending claims 1-8 could not have been rendered obvious in a manner alleged in these rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

As to the objection of claims 10 and 12 as well as the rejections involving claims 9-13, they have been rendered moot in view of the canceling of these claims. It is submitted, however, agreeing to the canceling of these claims should not be construed as acquiescence with regard to the merits of any such rejections directed thereto.

It is submitted neither Kamikuri et al nor Winslow et al, either separately or in combination, would have led to achieving the present invention such as according to claims 1+. Kamikuri et al disclosed a semiconductor device which is flip-chip bonded to a wiring board. For example, with regard to the stacked structure shown in Fig. 1 of the drawings thereof, bumps 35 which are for flip-chip bonding are formed on a front surface of a semiconductor element 33. The bumps 35 are bond-connected to the wirings 39 on the wiring board 37. The face-down electrical connection of the semiconductor element 33 to the wiring board 37 is a flip-chip mounting scheme. Other such mounting arrangements are shown in connection with Figs. 2-3 in Kamikuri et al.

Winslow et al disclosed a dual band power amplifier scheme having improved isolation. An example of this is shown in connection with Figs. 1-3 thereof in which separate dies 14a and 14b include a high-band power amplifier and a low-band power amplifier, respectively. Winslow et al achieved low-band to high-band isolation through a filtered harmonic trapping scheme. It is also noted that in Winslow et al, the separate power amplifier dies are not in the vertical stacking arrangement.

Neither Kamikuri et al nor Winslow et al were concerned with the placement of individual circuits such as power circuits in chips which are to be mounted in the amplifier power module in the manner in which placement of the individual component circuits is prescribed as that now called for in independent claim 1 and, therefore, also in accordance with the dependent claims thereof. For at least these

reasons, the invention according to claims 1+ could not have been rendered obvious, as alleged in the outstanding rejection.

Hashemi et al was cited, allegedly, as teaching "an amplifier circuit allowing two or more frequency bands to be used." In this regard, column 3, lines 33-37, in Hashemi et al was specifically cited in support thereof. However, Hashemi et al's multi-band low noise amplifier scheme does not overcome the deficiencies of the combined teachings of Kamikuri et al and Winslow et al, insofar as the invention according to base claim 1 is concerned. In fact, there is no apparent evidence even over the combination of Kamikuri et al and Winslow et al that would have motivated one of ordinary skill to even consider combining the teachings of Kamikuri et al and Winslow et al. Therefore, for the same and similar reasons, the invention according to claim 2 is also considered patentable. It is submitted, the invention according to the corresponding dependent claims 4, 6 and 7, also could not have been rendered obvious, for the same and similar reasons.

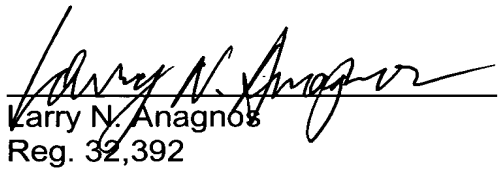
Concerning claims 1, 5 and 8, the combination of Lo et al and Winslow et al was applied in the outstanding rejection thereto. Lo et al also disclosed a package structure including a stacked arrangement of chips. It is submitted, however, Lo et al was not concerned with the positioning or placement of individual component circuits of the differently stacked chips such as that called for in claims 1, 2 and 8 of the drawings. Nor was Lo concerned with the problems addressed by the present inventors which led to achieving their invention. Also, there is no teaching in Winslow et al or, for that matter, even in view of the combined teachings of Winslow et al (discussed above) and Lo et al that would have led to the present invention.

At least for the above reasons, reconsideration and withdrawal of the outstanding objections/rejections and favorable action on the currently pending claims 1-8 as well as an early formal notification of allowability of the above-identified application is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned representative at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 1374.43628X00) and credit any excess fees to such deposit account.

Very truly yours,
Antonelli, Terry, Stout & Kraus, LLP



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